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Use of Oscillograph Records to Analyze System Performance

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Power System Analysis

Protection of present-day power systems is accomplished by a complex system of extremely sensitive relays that function only during a fault in the power system. Because relays are extremely fast, automatic oscillographs installed at appropriate locations can be used to determine the performance of protective relays during abnormal system conditions. Information from oscillographs can be used to detect the:

1. Presence of a fault
2. Severity and duration of a fault
3. Nature of a fault (A phase to ground, A – B phases to ground, etc.)
4. Location of line faults
5. Adequacy of relay performance
6. Effective performance of circuit breakers in circuit interruption
7. Occurrence of repetitive faults
8. Persistency of faults
9. Dead time required to dissipate ionized gases
10. Malfunctioning of equipment
11. Cause and possible resolution of a problem

Another important aspect of analyzing oscillograms is that of collecting data for statistical analysis. This would require a review of all oscillograms for every fault. The benefits would be to detect incipient problems and correct them before they become serious problems causing multiple interruptions or equipment damage.

An analysis of an oscillograph record shown in [Fig. 6.1](#) should consider the nature of the fault. Substation Y is comprised of two lines and a transformer. The high side winding is connected to ground. Oscillographic information is available from the bus potential transformers, the line currents from breaker A on line 1, and the transformer neutral current. An “A” phase-to-ground fault is depicted on line 1. The oscillograph reveals a significant drop in “A” phase voltage accompanied with a rise in “A” phase line 1 current and a similar rise in the transformer neutral current. The “A” phase breaker cleared the fault in 3 cycles (good). The received carrier on line 1 was “off” during the fault (good) permitting high-speed tripping at both terminals (breakers A and B). There is no evidence of AC or DC current transformer (CT) saturation of either the phase CTs or the transformer neutral CT. The received carrier

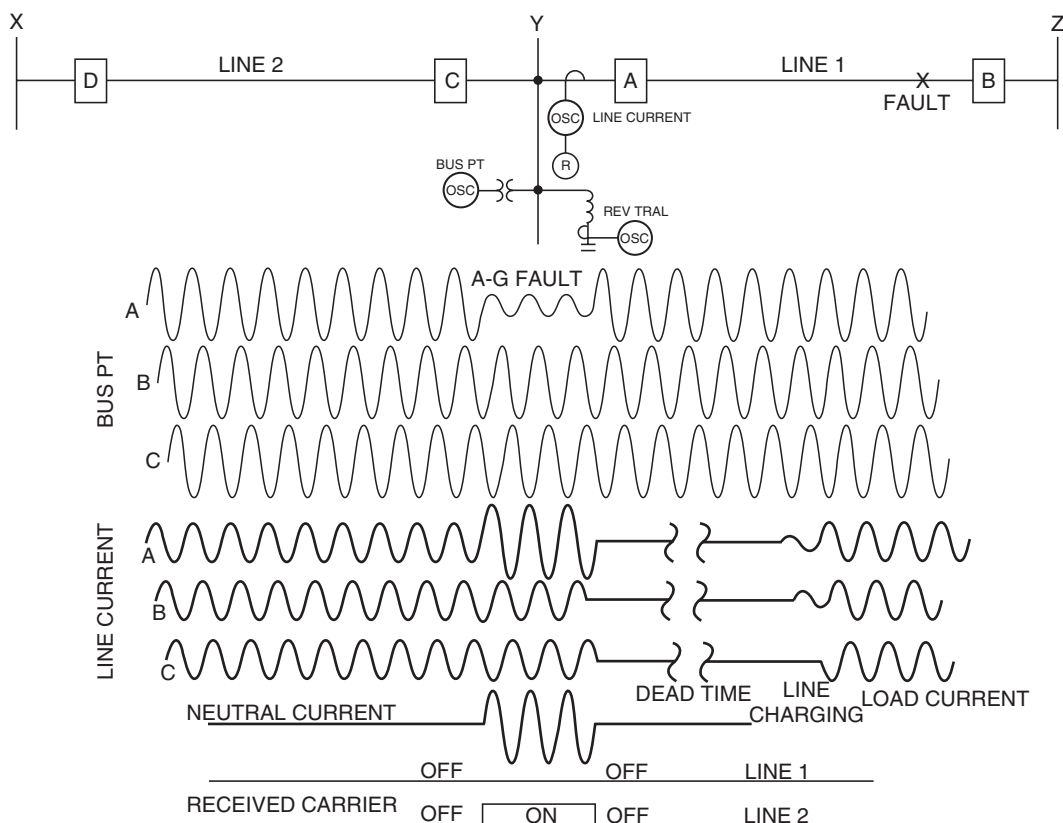


FIGURE 6.1 Analysis of an oscillograph record.

signal on line 2 was “on” all during the fault to block breaker “D” from tripping at terminal “X”. This would indicate that the carrier ground relays on the number 2 line performed properly. This type of analysis may not be made because of budget and personnel constraints. Oscillographs are still used extensively to analyze known cases of trouble (breaker failure, transformer damage, etc.), but oscillograph analysis can also be used as a maintenance tool to prevent equipment failure.

The use of oscillograms as a maintenance tool can be visualized by classifying operations as good (A) or questionable (B) as shown in Fig. 6.2. The first fault current waveform (upper left) is classified as A because it is sinusoidal in nature and cleared in 3 cycles. This could be a four or five cycle fault clearing time and still be classified as A depending upon the breaker characteristics (4 or 5 cycle breaker, etc.) The DC offset wave form can also be classified as A because it indicates a four cycle fault clearing time and a sinusoidal waveform with no saturation.

An example of a questionable waveform (B) is shown on the right side of Fig. 6.2. The upper right is one of current magnitude which would have to be determined by use of fault studies. Some breakers have marginal interrupting capabilities and should be inspected whenever close-in faults occur that generate currents that approach or exceed their interrupting capabilities. The waveform in the lower right is an example of a breaker restrike that requires a breaker inspection to prevent a possible breaker failure of subsequent operations.

Carrier performance on critical transmission lines is important because it impacts fast fault clearing, successful high-speed reclosing, high-speed tripping upon reclosure, and delayed breaker failure response for permanent faults upon reclosure, and a “stuck” breaker. In Fig. 6.3 two waveforms are shown that depict adequate carrier response for internal and external faults. The first waveform shows a

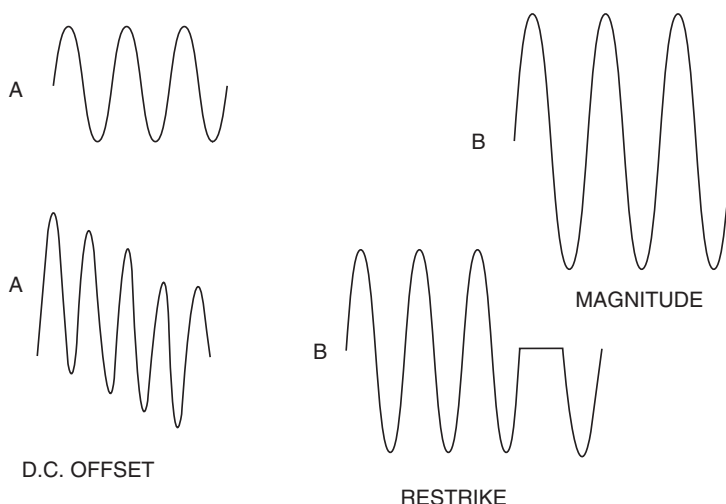


FIGURE 6.2 Use of oscillograms as a maintenance tool.

3 cycle fault and its corresponding carrier response. A momentary burst of carrier is cut off quickly allowing the breaker to trip in 3 cycles. Upon reclosing, load current is restored. The bottom waveform depicts the response of carrier on an adjacent line for the same fault. Note that carrier was “off” initially and cut “on” shortly after fault initiation. It stayed “on” for a few cycles after the fault cleared and stayed “off” all during the reclose “dead” time and after restoration of load current. Both of these waveforms would be classified as “good” and would not need further analysis.

An example of a questionable carrier response for an internal fault is shown in Fig. 6.4. Note that the carrier response was good for the initial 3 cycle fault, but during the reclose dead time, carrier came back “on” and was “on” upon reclosing. This delayed tripping an additional 2 cycles. Of even greater concern is a delay in the response of breaker-failure clearing time for a stuck breaker. Breaker failure initiation is predicated upon relay initiation which, in the case shown, is delayed 2 cycles. This type of “bad” carrier

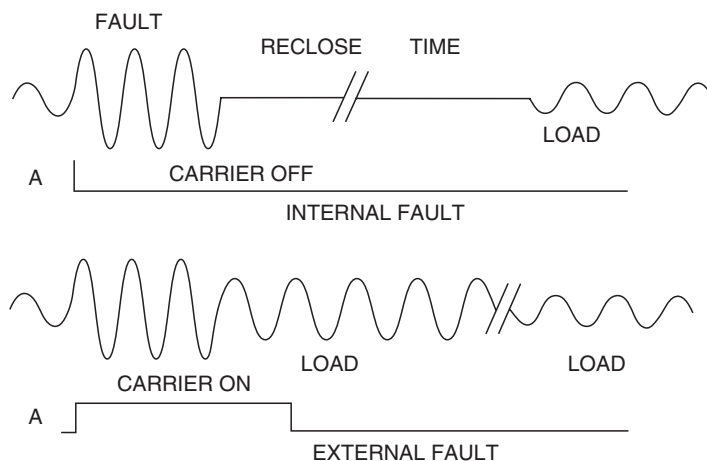


FIGURE 6.3 Two waveforms that depict adequate carrier response for internal and external faults.

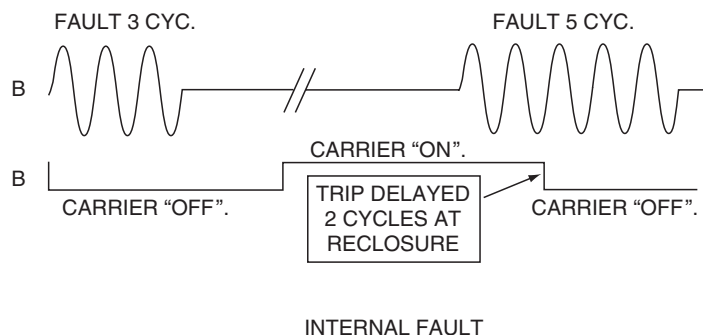


FIGURE 6.4 A questionable carrier response for an internal fault.

response may go undetected if oscillograms are not reviewed. In a similar manner, a delayed carrier response for an internal fault can result in delayed tripping for the initial fault as shown in Fig. 6.5. However, a delayed carrier response on an adjacent line can be more serious because it will result in two or more line interruptions. This is shown in Fig. 6.6. A fault on line 1 in Fig. 6.1 should be accompanied by acceptable carrier blocking signals on all external lines that receive a strong enough signal to trip if not accompanied by an appropriate carrier blocking signal. Two conditions are shown. A good (“A”) block signal and questionable (“B”) block signal. The good block signal is shown as one that blocks (comes “on”) within a fraction of a cycle after the fault is detected and unblocks (goes “off”) a few cycles after the fault is cleared. The questionable block signal shown at the bottom of the waveform in Fig. 6.6 is late in going from “off” to “on” (1.5 cycles). The race between the trip element and the block element is such that a trip signal was initiated first and breaker “D” tripped 1.5 cycles after the fault was cleared by breaker A in 3 cycles. This would result in a complete station interruption at station “Y.”

Impedance relays receive restraint from either bus or line potentials. These two potentials behave differently after a fault has been cleared. This is shown in Fig. 6.7. After breakers “A” and “B” open and the line is deenergized, the bus potential restores to its full value thereby applying full restraint to all impedance relays connected to the bus. The line voltage goes to zero after the line is deenergized. Normally this is not a problem because relays are designed to accommodate this condition. However, there are occasions when the line potential restraint voltage can cause a relay to trip when a breaker recloses. This condition usually manifests itself when shunt reactors are connected on the line. Under these conditions an oscillatory voltage will exist on the terminals of the line side potential devices after

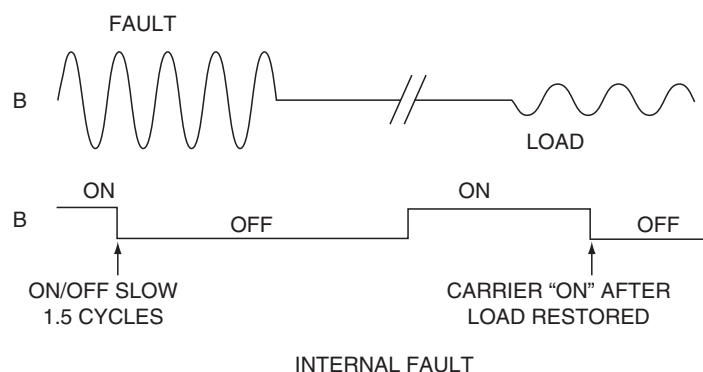


FIGURE 6.5 A delayed carrier response for an internal fault that resulted in delayed tripping for the initial fault.

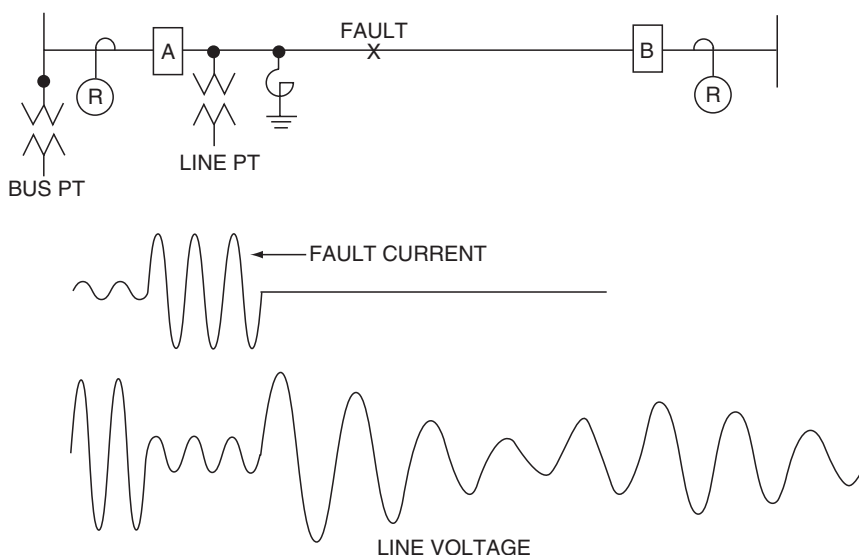
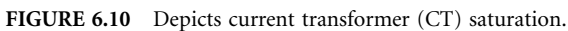
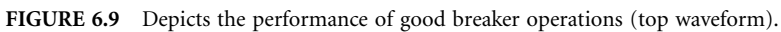


FIGURE 6.8 A waveform example after both “A” and “B” breakers have been opened.

results in oscillations that are mirror images of each other. The voltage on the center phase is usually a constant decaying decrement. These oscillations can last up to 400 cycles or more. This abnormal voltage is applied to the relays at the instant of reclosure and has been known to cause a breaker (for example, “A”) to trip because of the lack of coordination between the voltage restraint circuit and the overcurrent monitoring element. Another more prevalent problem is multiple restrikes across an insulator during the oscillatory voltage on the line. These restrikes prevent the ionized gasses from dissipating sufficiently at the time of reclosure. Thus a fault is reestablished when breaker “A” and/or “B” recloses. This phenomena can readily be seen on oscillograms. Action taken might be to look for defective insulators or lengthen the reclose cycle.

The amount of “dead time” is critical to successful reclosures. For example, at 161 kV a study was made to determine the amount of dead time required to dissipate ionized gasses to achieve a 90% reclose success rate. In general, on a good line (clean insulators), at least 13 cycles of dead time are required. Contrast this to 10 cycles dead time where the reclose success rate went down to approximately 50%. Oscillograms can help determine the dead time and the cause of unsuccessful reclosures. Note the dead time is a function of the performance of the breakers at both ends of the line. [Figure 6.9](#) depicts the performance of good breaker operations (top waveform). Here, both breakers trip in 3 cycles and reclose successfully in 13 cycles. The top waveform depicts a slow breaker “A” tripping in 6 cycles. This results in an unsuccessful reclosure because the overall dead time is reduced to 10 cycles. Note, the oscillogram readily displays the problem. The analysis would point to possible relay or breaker trouble associated with breaker “A.”

[Figure 6.10](#) depicts current transformer (CT) saturation. This phenomenon is prevalent in current circuits and can cause problems in differential and polarizing circuits. The top waveform is an example of a direct current (DC) offset waveform with no evidence of saturation. That is to say that the secondary waveform replicates the primary waveform. Contrast this with a DC offset waveform (lower) that clearly indicates saturation. If two sets of CTs are connected differentially around a transformer and the high side CTs do not saturate (upper waveform) and the low side CTs do saturate (lower waveform), the difference current will flow through the operate coil of the relay which may result in deenergizing the transformer when no trouble exists in the transformer. The solution may be the replacement of the offending low side CT with one that has a higher “C” classification, desensitizing the relay or reducing



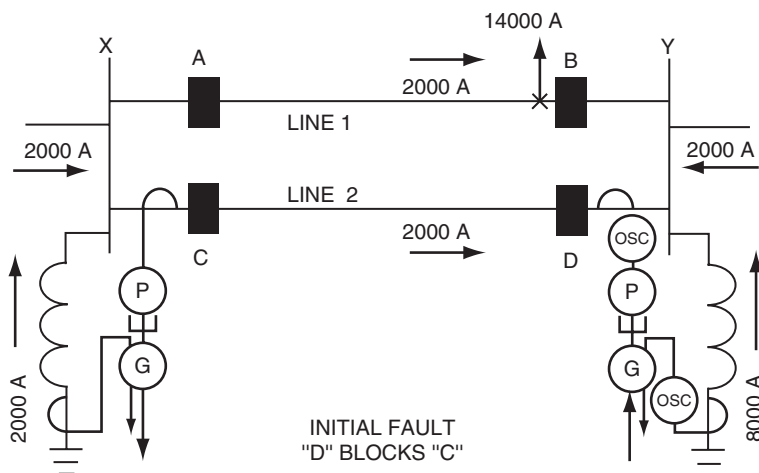


FIGURE 6.11 A line 1 fault at the terminals of breaker “B.” Figures 6.11 through 6.14 demonstrate step-by-step sequence.

the magnitude of the fault current. Polarizing circuits are also adversely affected by CTs that saturate. This occurs where a residual circuit is compared with a neutral polarizing circuit to obtain directional characteristics and the apparent shift in the polarizing current results in an unwanted trip.

Current reversals can result in an unwanted two-line trip if carrier transmission from one terminal to another does not respond quickly to provide the desired block function of a trip element. This is shown in a step-by-step sequence in Figs. 6.11 through 6.14. Consider a line 1 fault at the terminals of breaker “B” (Fig. 6.11). For this condition, 2000 amperes of ground fault current is shown to flow on each line from terminal “X” to terminal “Y.” Since fault current flow is towards the fault at breakers “A” and “B”, **neither** will receive a signal (carrier “off”) to initiate tripping. However, it is assumed that both breakers do not open at the same time (breaker “B” opens in 3 cycles and breaker “A” opens in 4 cycles). The response of the relays on line 2 is of prime concern. During the initial fault when breakers “A” and “B” are both closed, a block carrier signal must be sent from breaker “D” to breaker “C” to prevent the tripping of breaker “C.” This is shown as a correct “on” carrier signal for 3 cycles in the bottom

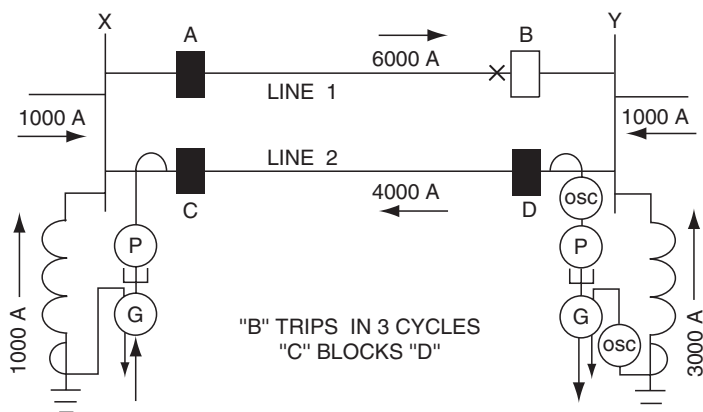


FIGURE 6.12 Second step in sequence.

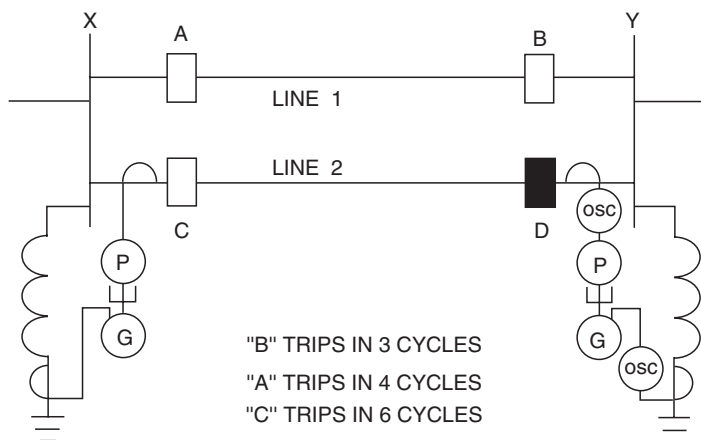


FIGURE 6.13 Third step in sequence.

oscillogram trace in Fig. 6.14. However, when breaker "B" trips in 3 cycles, the fault current in line 2 increases to 4000 amperes and, more importantly, it reverses direction to flow from terminal "Y" to terminal "X." This instantaneous current reversal requires that the directional relays on breaker "C" pickup to initiate a carrier block signal to breaker "D." Failure to accomplish this may result in a trip of breaker "C" if its own carrier signal does not rise rapidly to prevent tripping through its previously made up trip directional elements. This is shown in Fig. 6.13 and oscillogram record Fig. 6.14. An alternate

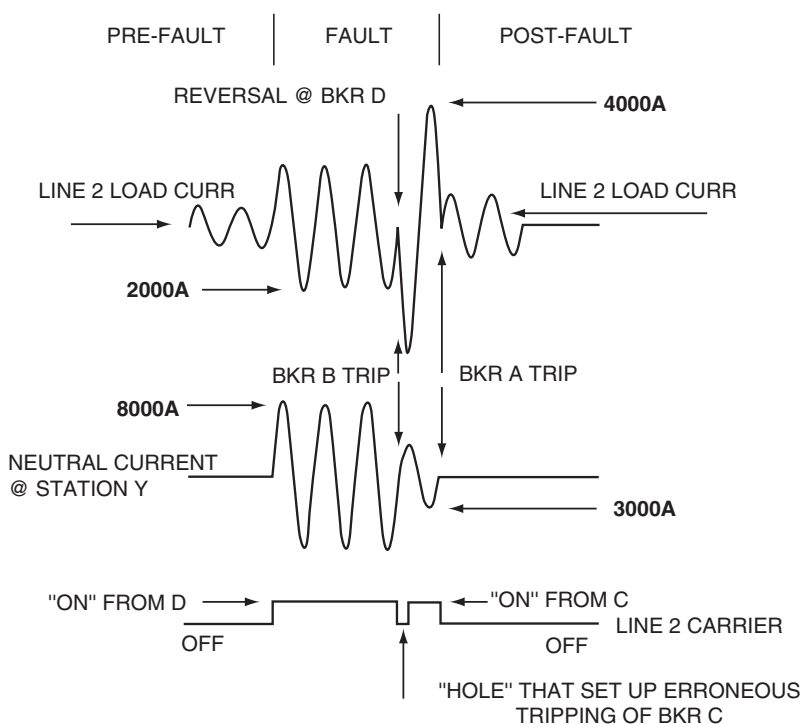


FIGURE 6.14 Final step in sequence.

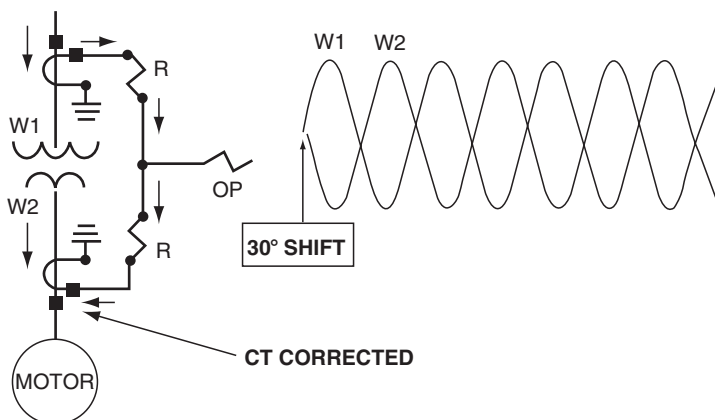


FIGURE 6.17 Corrected connection.

in Fig. 6.15. The upper waveform restrike sequence depicts a 1/2 cycle restrike that is successfully extinguished within the interrupter. The lower waveform depicts a restrike that goes around the interrupter. This restrike cannot be extinguished and will last until the oil becomes badly carbonized and a subsequent fault occurs between the bus breaker terminal and the breaker tank (ground). In Fig. 6.15 the interrupter bypass fault lasted 18 cycles. Depending upon the rate of carbonization, the arc time could last longer or less before the flashover to the tank. The result would be the same. A bus fault that could have devastating affects. One example resulted in the loss of eight generators, thirteen 161 kV lines, and three 500-kV lines. The reason for the extensive loss was the result of burning oil that drifted up into adjacent busses steel causing multiple bus and line faults that deenergized all connected equipment in the station. The restrike phenomena is a result of a subsequent lightning strikes across the initial fault (insulator). In the example given above, lightning arresters were installed on the line side of each breaker and no additional restrikes or breaker failures occurred after the initial destructive failures.

Oscillography in microprocessor relays can also be used to analyze system problems. The problem in Fig. 6.16 involves a microprocessor differential relay installation that depicts the failure to energize a large motor. The CTs on both sides of the transformer were connected wye-wye but the low side CTs were rolled. The 30° shift was corrected in the relay and was accurately portrayed by oscillography in the microprocessor relay but the rolled CTs produced current in the operate circuit that resulted in an erroneous trip. Note that with the low side CTs rolled, the high and low side currents W1 and W2 are in phase (incorrect). The oscillography output clearly pin-pointed the problem. The corrected connection is shown in Fig. 6.17 together with the correct oscillography (W1 and W2 180° out of phase).

